REMARKS

This is a full and timely response to the non-final Official Action mailed **August 27, 2003** (Paper No. 2). Reconsideration of the application in light of the above amendments and the following remarks is respectfully requested.

By the forgoing amendment, claims 1 and 20 have been amended. Additionally, new claims 26-41 have been added, and original claims 10-19, 24 and 25 have been cancelled. Thus, claims 1-9, 20-23 and 26-41 are currently pending for the Examiner's consideration.

The only issues raised in the Office Action were rejections based on cited prior art. Specifically, claims 1-9, 11-23 and 25 were rejected as anticipated under 35 U.S.C. § 102(b) by U.S. Patent No. 5,184,091 to Srivastava ("Srivastava"). Claims 10 and 24 were rejected as being unpatentable under 35 U.S.C. § 103(a) over the combined teachings of Srivastava and U.S. Patent No. 5,473,385 to Leske ("Leske").

By the present amendment, claim 1 is amended to include the recitations of canceled claim 10. Claim 20 is amended to include the recitations of canceled claim 24. Therefore, the rejections of claims 10 and 24 now applied respectively to claims 1 and 20 and are respectfully traversed for at least the following reasons.

Claim 1 recites:

> An apparatus for outputting a clock signal for video reconstruction in a terminal, comprising:
> an oscillator that generates the clock signal;
> a control logic circuit with a phase locked loop for receiving an incoming video signal and phase locking to a clock signal portion of the incoming video signal, wherein the control logic circuit outputs a control signal for controlling an output of the oscillator based on the phase lock; and
> a frequency range bounder in the phase locked loop that receives the control signal and outputs a bounded control signal that bounds the frequency of the oscillator to a selected range;

wherein the incoming video signal is a digital signal and the clock signal portion of the incoming video signal is program clock reference data for the digital signal.

(emphasis added).

Claim 20 recites similar subject matter in the form of a method claim.

The recent Office Action concedes that Srivastava fails to teach or suggest bounding the frequency range of an oscillator in a digital video system used for video reconstruction. (Paper No. 2, page 6). Consequently, the Office Action cited Leske which merely "teaches that the MPEG standards provide for an MPEG transport stream that includes . . . 'program clock reference' (PCR) structures." (*Id.*) According to the Office Action, "it would have been obvious . . . to incorporate the program clock reference data for the digital signal taught by Leske into Srivastava's system in order to adjust a decoding clock to accommodate mismatches between its frequency and the frequency of an encoding clock in response to video synchronization signals in the digital video signal." (*Id.*)

However, there is nothing in the cited prior art that suggests such a combination. Srivastava does not indicate or suggest that the methods disclosed can be applied to a digital video system. Such a teaching or suggestion comes only from Applicant's own specification.

"The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. In re Mills, 916 F.2d 680, 16 USPQ2d 1420 (Fed. Cir. 1990)." M.P.E.P. § 2143.01. "Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally

available to one of ordinary skill in the art. In re Fine, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); In re Jones, 958 F.2d 347, 21 USPQ2d 1941 (Fed Cir. 1992)." M.P.E.P. § 2143.01 (emphasis added). Consequently, the rejection of claims 1-9 and 20-23 should be reconsidered and withdrawn.

Additionally, several of the original dependent claims recite subject matter that is not taught or suggested by the prior art of record. For example, consider claims 4-8.

Claim 4 recites "wherein the frequency range bounder includes an output multiplexer that selects one of the upper value, the control signal, and the lower value as the bounded control signal and outputs the bounded control signal to the oscillator to bound the oscillator frequency between an upper level and a lower level."

In contrast, Srivastava does not teach or suggest three signals (upper, lower and control) where one of the signal is selected "as the bounded control signal" and output to the oscillator. Rather, Srivastava teaches a circuit in which the control signal (from the error amplifier 55) is always output to the oscillator (104). Based on several different thresholds, implemented by the threshold detector (60) and the limit detector (70), a correction signal may be generated and added to the control signal at summer (100) before the control signal is provided to the oscillator (104). However, Srivastava does not teach or suggest three signals where only one of the three is selected for transmission to the oscillator.

Claim 5 additionally recites: "wherein the frequency range bounder includes at least one of a high comparator and a low comparator coupled to the output multiplexer, wherein the high comparator compares the control signal with a high limit and the low comparator compares the control signal with a low limit, and wherein the output multiplexer outputs the

upper value as the bounded control signal if the control signal is above the high limit and outputs the lower value as the bounded control signal if the control signal is below the low limit." These features are neither taught nor suggested by Srivastava

Claim 6 recites "wherein the frequency range bounder includes at least one of a minimum function block coupled to the high limit register and a maximum function block coupled to the low limit register, wherein the minimum function block outputs the smaller of the control signal and the upper value and wherein the maximum function block outputs the larger of the control signal and the lower value as the bounded control signal." Srivastava does not teach or suggest anything similar to this arrangement in which two successive function blocks each compare two signals and selectively pass one of the two on to ultimately produce a control signal for an oscillator. As indicated above, Srivastava rather operates a number of counters (63, 123) to generate a correction that is added to a control signal from a phase detector (50).

Claim 7 recites: "wherein the frequency range bounder includes a comparator coupled to the high limit register and low limit register, wherein the comparator compares the control signal with the upper and lower values and outputs the control signal to the output register if the control signal is between the upper and lower values." In contrast, Srivastava does not teach or suggest a comparator that receives and compares the control signal to high and low values and potentially outputs *the same control signal*. Rather, Srivastava teaches a comparator (60) that *never* outputs the control signal, only operates a counter (63) in response to the control signal.

"A claim is anticipated [under 35 U.S.C. § 102] only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art

reference." Verdegaal Bros. v. Union Oil Co. of California, 2 U.S.P.Q.2d 1051, 1053 (Fed. Cir. 1987) (emphasis added). See M.P.E.P. § 2131. For at least these reasons, claims 4-8 are clearly patentable over Srivastava.

The newly added claims 26-41 recite subject matter that is similar to that recited in claims 4-8. Consequently, new claims 26-41 are patentable over the prior art of record, particularly Srivastava, for at least the reasons given above with reference to claims 4-8. Examination and allowance of new claims 26-41 is respectfully requested.

For the foregoing reasons, the present application is thought to be clearly in condition for allowance. Accordingly, favorable reconsideration of the application in light of these remarks is courteously solicited. If any fees are owed in connection with this paper which have not been elsewhere authorized, authorization is hereby given to charge those fees to Deposit Account 18-0013 in the name of Rader, Fishman & Grauer PLLC. If the Examiner has any comments or suggestions which could place this application in even better form, the Examiner is requested to telephone the undersigned attorney at the number listed below.

Respectfully submitted,

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